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Setting Out to Explore of XOR/XNOR Gates in conjunction with Adiabatic Expertise

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ABSTRACT

The most commonly used arithmetic operation is addition and it is the speed- limiting element to make faster VLSI processors. As the demand for higher performance processors grows, there is a need to improve arithmetic unit performance. The aim of the project is to reduce the power consumption and delay of full adder circuit. The six new hybrid 1-bit full-adder (FA) circuits based on the novel full-swing XOR–XNOR or XOR/XNOR gates. Each of the planned circuits has its own deserves in terms of speed, power consumption, power delay product (PDP), driving ability, and so on. The proposed system uses a new low power logic called ADIABATIC LOGIC which reduces the power and delay of the existed circuits. The word ADIABATIC is derived from the Greek word ADIABATOS which means there is no exchange of energy with the environment and hence no energy loss in form of heat dissipation. Adiabatic logic is the term given to low power electronics circuits that implement reversible logic. Adiabatic logic is commonly used to reduce the energy loss during the charging and discharging process of circuit operations. Adiabatic logic is also known as energy recovery or charge recovery logic. The adiabatic logic structure dramatically reduces power dissipation. Simulations with Tanner 16.0 tool confirm the superiority of the proposed cells compared with the previously reported ones in terms of power and delay.

Keywords— **VLSI, logic gates, Adiabatic Technology, simulation**

I.INTRODUCTION

The explosive growth in a laptop computer, transportable systems, and cellular networks has intense analysis efforts in low-power electronics. Today, there is an ever- increasing number of portable applications requiring low power and high throughput circuits. Therefore, low-power design has become a major design consideration [1]. The adder is one of the most critical components of a processor, as it is used in the arithmetic logic unit (ALU), in the floating-point unit, and for address generation in case of cache or memory access [2].

The full adder performance would have an effect on the system as an entire. A variety of full adders using static or dynamic logic styles have been reported in the literature [3]. In total, we have found 34 different full adder

implementations. The conventional adder uses twenty-eight transistors enforced in CMOS technique.

A new full adder referred to as static energy-recovery full-adder (SERF) uses solely ten transistors, which has the least number of transistors and has reported to be the best in power consumption, according to [4]. Many low-power adders apply circuit-level techniques using various pass transistors, such as the SERF [5].

Compared to the complementary static CMOS adders, such low-power adders have the problem of threshold loss, i.e., the logic value 1 is not the value of 1 and the logic value 0 may not be the value of 0 volts.

II.OVERVIEW

Fig: 1 Static CMOS logic circuit

devices like mobile phones, personal digital assistants (PDAs) and notebooks demand VLSI and ultra-large-scale integration designs with an enhanced power delay characteristics. Full adders, being one of the most basic building blocks of all the prior circuit applications, remain a vital focus domain of the researchers over the years. Different logic styles, each having its own merits and impediment, was investigated to implement1-bit full adder cells. The designs, reported so far, may be broadly classified into two categories: 1) static style and 2) dynamic style.
Different logic styles tend to favor one performance aspect at the expense of others. Standard static Complementary Metal– Oxide–Semiconductor (CMOS) dynamic CMOS logic Complementary Pass-Transistor Logic (CPL) and Transmission Gate Full Adder (TGA) are the most important logic design styles in the conventional domain. The other adder designs use more than one logic style, known as hybrid-logic design style, for their implementation. These designs exploit the features of different logic styles to improve the overall performance of the full adder.

In this paper, we evaluate several circuits for the XOR or XNOR (XOR/XNOR) and simultaneous XOR and XNOR (XOR–XNOR) gates and offer new circuits for each of them. Also, we try to remove the problems existing in the investigated circuits. Afterward, with these new XOR/XNOR and XOR–XNOR circuits, we have a tendency to propose six new FA structures. In this project we overcome the drawbacks of those six new FA structures using ADIABATIC LOGIC GATES. These six full adder [8] structures are designed using XOR/XNOR circuits can be developed by using two different design methodologies which are Static logic and Dynamic logic.

Static logic is a design methodology in integrated circuit design where there is at all times some mechanism to drive the output either high or low was described in Fig: 1. For example, in many of the popular logic families, such as TTL and traditional CMOS, there is always a low- impedance path between the output and either the supply voltage or the ground. The most widely used logic style is static CMOS. A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN). The basic construction of a Two input Static CMOS XOR/XNOR logic gates is shown in Fig: 2. The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0 (based on the inputs). The PUN and PDN networks are constructed in a mutually exclusive fashion such

that, one and only one of these networks is conducting in the steady state.

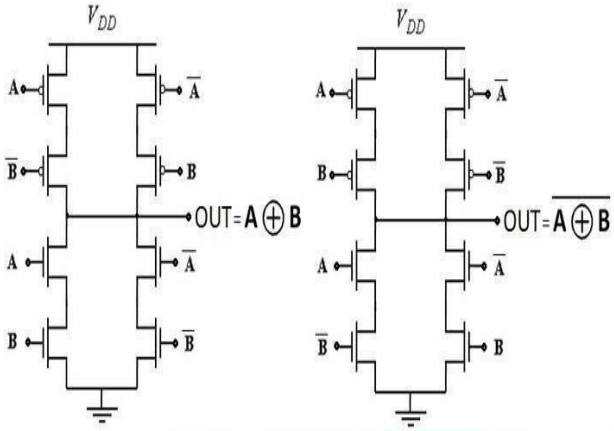


Fig: 2 Two input Static CMOS XOR/XNOR logic gates

Dynamic CMOS Logic

Dynamic logic is a design methodology in integrated circuit design in that it uses a clock signal in its implementation of combinational logic circuits. In dynamic logic, there is not always a mechanism driving the output high or low. In the most common version of this concept, the output is driven high or low during distinct parts of the clock cycle. Dynamic logic requires a minimum clock rate fast enough that the output state of each dynamic gate is used before it leaks out of the capacitance holding that state. The basic construction of a dynamic logic gate is shown in Fig: 3. The PDN (pull-down network) is constructed exactly as in complementary CMOS. The operation of this circuit is divided into two major phases: pre-charge and evaluation, with the mode of operation determined by the clock signal CLK

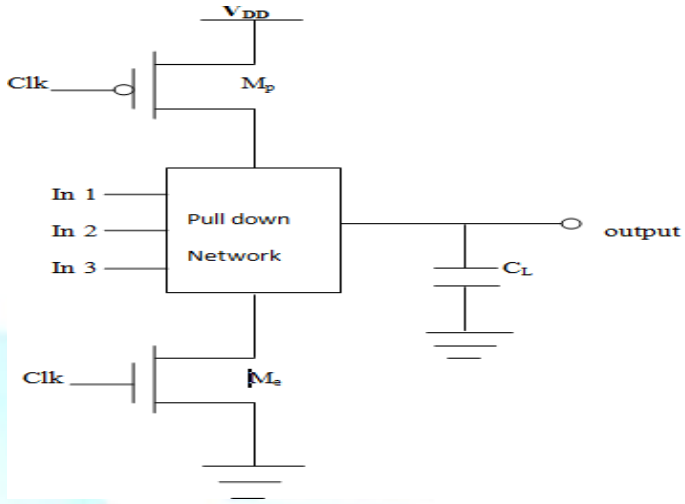


Fig: 3 Dynamic CMOS logic circuit

Pre-charge: When CLK = 0, the output node Out is pre-charged to VDD by the PMOS transistor Mp. During that time, the evaluate NMOS transistor Me is off, so that the pull-down path is disabled. The evaluation FET eliminates any static power that would be consumed during the pre-charge period (this is, static current would flow between the supplies if both the pull down and the pre-charge device were turned on simultaneously).

Evaluation: For CLK = 1, the pre-charge transistor Mp is off, and the evaluation transistor Meis turned on. The output is conditionally discharged based on the input values and the pull-down topology. If the inputs are such that the PDN conducts, then a low resistance path exists between Out and GND and the output is discharged to GND. If the PDN is turned off, the pre-charged value remains stored on the output capacitance CL, which is a combination of junction capacitances, the wiring capacitance, and the input capacitance of the fan-out gates.

During the evaluation phase, the only possible path between the output node and a supply rail is to GND. Consequently, once Out is

discharged, it cannot be charged again till then next pre-charge operation. The inputs to the gate can therefore make at most one transition during evaluation.

LOGICS IN DESIGN OFLOWPOWER

CPL Logic (complementary pass transistorlogic)

Every CPL has two output wires, both the positive signal and the complementary signal, eliminate in the need for inverters. Complementary pass transistor logic or differential pass transistor logic refers to logic family which is designed for certain advantage.

Transmission Gate (TG) Logic

A transmission gate is similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is a CMOS based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1.both PMOS and NMOS work simultaneously.

DPL Logic (Double pass transistor logic)

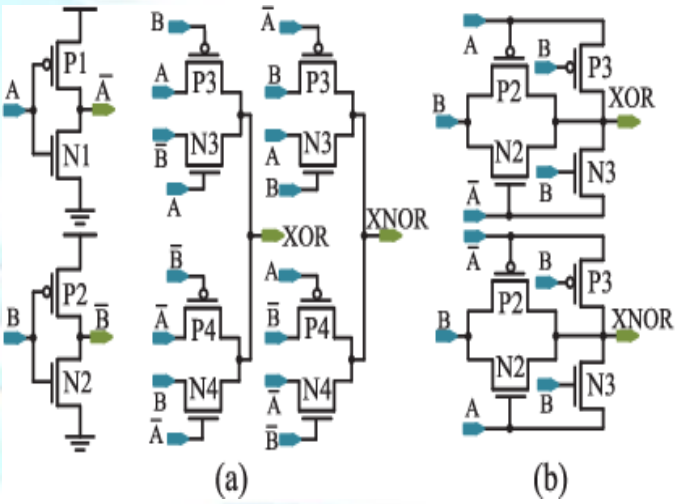
Double pass transistor logic (DPL) is a modified version of complementary pass transistor logic (CPL) that meets the requirement of reduced supply voltage designs In DPL circuits full swing operation is achieved by simply adding PMOS transistors in parallel with the NMOS transistors.

PTL Logic (Pass transistor logic)

In electronics, pass transistor logic describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant [7] transistors.

PSO Algorithm

The PSO algorithm maintains multiple potential solutions at one time. During each Iteration algorithm, each solution is evaluated by an objective function to determine its fitness. Each solution represented by a particle in the fitness landscape (search space). The particle "Fly" or "swarm" through the search space to find the maximum value returned by objective function.



III. EXISTINGSYSTEM

REVIEW OF XOR/XNORGATES

Hybrid FAs are made of two modules, including 2-input XOR/XNOR (or simultaneous XOR–XNOR) gate and 2-to-1 multiplexer (2-1-MUX) gate. The XOR/XNOR gate is the major consumer of power in the FA cell. Therefore, the power consumption of the FA cell can be reduced by optimum designing of the XOR/XNOR gate. The XOR/XNOR gate has also many applications in digital circuits design. Many circuits have been proposed to implement XOR/XNOR gate [6] which a few examples of the most efficient ones are shown in Fig: 4.It shows the full-swing XOR/XNOR gate circuit

designed by Double Pass-Transistor [9] Logic (DPL) style. This structure has eight transistors.

The main problem of this circuit is using two high power consumption NOT gates on the critical path of the circuit, because the NOT gates must drive the output capacitance. Therefore, the size of the transistors in the NOT gates should be increased to obtain lower critical path delay. Furthermore, it causes the creation of an intermediate node with a large capacitance. Of course, this means that the NOT gates drives the output of circuit through, for example, pass transistor or TG. Therefore, the short-circuit power and, thus, the total power dissipation of this circuit are widely Increased. Moreover, in the optimum PDP situation, the critical path delay will also be increased slightly.

One of the most important issues in VLSI design is power consumption. With continuously increasing chip complexity and number of transistors in a chip, circuit's power consumption is growing as well. Higher power consumption raises chip temperature and directly affects battery life in portable devices as it causes more current to be withdrawn from the power supply. High temperature afflicts circuit operation and reliability.

Fig : 4 (a) Full-swing XOR (b) Full-swing XNOR

The drawbacks of existing system are as follows:

- More Power Consumption
- More Critical Path Delay
- High short-circuit power dissipation.

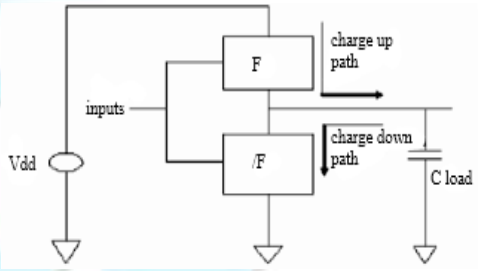
IV. PROPOSEDTECHNIQUE

In this paper, we evaluate several circuits for the XOR or XNOR (XOR/XNOR) and simultaneous XOR and XNOR (XOR–XNOR) gates and offer new circuits for each of them. Also, we try to remove the problems existing in the investigated circuits of six new full adder structures.

Afterward, with these new XOR/XNOR and XOR–XNOR circuits, with adiabatic logics are proposed to reduce the power consumption and also to reduce the delay compares to the existed full adder structures. In this project we proposed a new full adder with ADIABATIC LOGIC gates which is designed by taking the efficient full adder among the existed six new full adder structures.

ADIABATICTECHNOLOGY

The word ADIABATIC is derived from the



Greek word ADIABATOS which means there is no exchange of energy with the environment and hence no energy loss in form of heat dissipation. The term "adiabatic" describe the thermo dynamic processes in which no energy exchange with the environment, and therefore no dissipated energy loss. But in VLSI, the electric charge transfer between nodes of a

circuit is considered as the process and various techniques can be applied to minimize the energy loss during charge transfer event.

Fully adiabatic operation of a circuit is an ideal condition. It may be only achieved with very slow switching speed. In practical cases, energy dissipation with a charge transfer event is composed of an adiabatic component and a non-adiabatic component.In conventional CMOS logic circuits, from 0 to VDD transition of the output node, The total output energy $C_{LDD}V_D^2$ is drawn from power supply. At the end of transition, only $I^2C\ V^2$ energy is stored at the load capacitance. The half of drawn energy from power supply is dissipated in PMOS network (F). From VDD to 0 transition of the output node, energy stored in the load capacitance is dissipated in the NMOS network (/F).

Adiabatic logic circuits reduce the energy dissipation during switching process, and reuse some of energy by recycling from the load capacitance. For recycling, the adiabatic circuits use the constant current source power supply and for reduce dissipation it uses the trapezoidal or sinusoidal power supply voltage, Fig 5a,5b shows a basic adiabatic gate Adiabatic Circuits reduce dissipation by following key rules:

Never turn on a transistor when there is a voltage potential between source & drain.

Never turn off a transistor when current is flowing through it.

Fig 5a Basic adiabatic gate

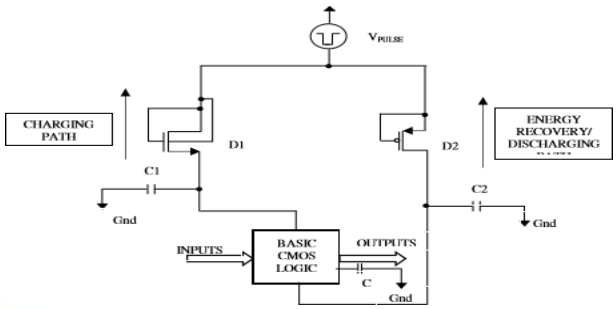


Fig 5b Basic circuit using adiabatic gate

Proposed Full Adder

The proposed full adder is designed to overcome the drawbacks in the existed method. In the existed system six new full adder structures are proposed using new XOR and XNOR circuits out of those six FA structures the HFA19T full adder structure has less power consumption and less delay compared to other five FA structures. But in the XOR circuit we use a inverter which drive the output of XOR circuit to other pipelined gates in the circuit. The inverter gate consumes more power in entire full adder [10] structure and offers delay in the output. To reduce these drawbacks and achieve more efficient results we use Adiabatic technology and proposed a Full Adder using new XOR and XNOR gates with the adiabatic technology.

Schematic Diagram of Proposed Full Adder

The proposed Full Adder schematic diagram is shown in the Fig 6a. In this proposed circuit the inverter gate which consumes more power in entire structure is designed using two level adiabatic logic (2LAL). The basic gate of 2LAL, a pair of transmission gates which transmit signal *A* and */A* respectively which is shown in Fig: 6b. The fact that 2LAL only

requires a basic switching device and is not dependent on CMOS makes it ideal for use with new technologies. Another feature of 2LAL is that inverters can be easily created by simply crossing over the rails when going from one gate to the next. Hence by using this 2LAL inverter we can reduce the power consumption and as well as we can reduce the delay at the output.

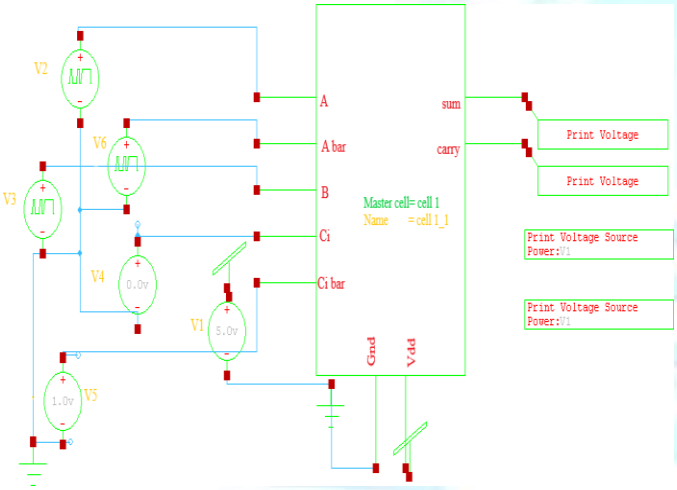


Fig: 6a Schematic of proposed Full Adder

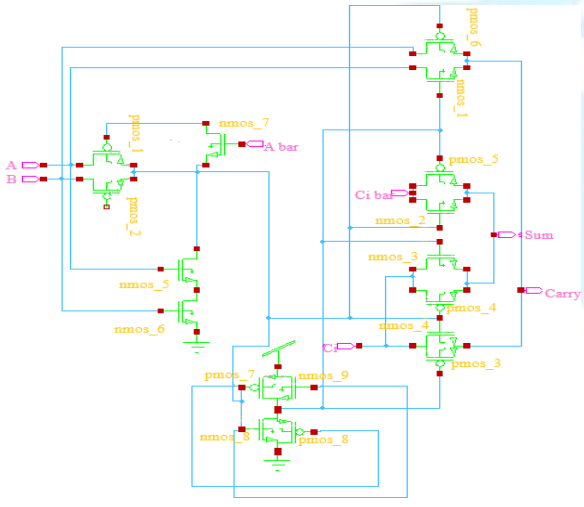


Fig: 6b Proposed Full Adder using adiabatic logic inverter

V.CONCLUSION

In this paper, we first evaluated the XOR/XNOR and XOR–XNOR circuits. The evaluation revealed that using the NOT gates on the critical path of a circuit is a drawback. Another disadvantage of a circuit is to have a positive feedback on the outputs of the XOR–XNOR gate for compensating the output voltage level. This feedback increases the delay, output capacitance, and as a result, energy consumption of the circuit. Then, we proposed new XOR/XNOR and XOR–XNOR gates that do not have the mentioned disadvantages. Finally, by using the proposed XOR and XOR–XNOR gates, we offered six new FA cells for various applications. Also, a modified method for transistor sizing in digital circuits was proposed. The new method utilizes the numerical computation PSO algorithm to select the appropriate size for transistors on a circuit and also it has very good speed, accuracy, and convergence. After simulating the FA cells in different conditions, the results demonstrated that the proposed circuits have a very good performance in all simulated conditions. Simulation results show that the proposed HFA-19T cell saves PDP up to 23. 4% compared with its best counterpart. Also, this cell has better speed and energy at all supply voltage ranges when is compared with other FA cells. To reduce more power consumption and delay in the circuit we proposed the HFA 19T circuit using Adiabatic Logic. With this proposed circuit we can reduce the PDP up to 25% compared with its best counterpart. Thus the full adder using adiabatic logic reduces the delay at the output.

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